

## **Marketing Bulletin**

- DATE: August 25, 2005
- TO: All Sales Personnel
- FROM: Mark Stoner
- **RE:** Product Termination

To all concerned parties,

This bulletin is to notify all customers of the discontinuation of the following Ecliptek series effective August 25<sup>th</sup>, 2005:

Series	Description	<b>Recommended Replacement</b>
E31J2	5V 6 pad SMD LVPECL VCXO	E32D1
E32J2	3.3V 6 pad SMD LVPECL VCXO	E32D1

In compliance with our End of Life (EOL) policy, this will serve as advanced notice of product termination. New orders will not be accepted after November 25<sup>th</sup>, 2005, with delivery to conclude by February 25<sup>th</sup> 2006.

If there are any questions pertaining to this bulletin, please fell free to contact me. Thank you again for your cooperation.

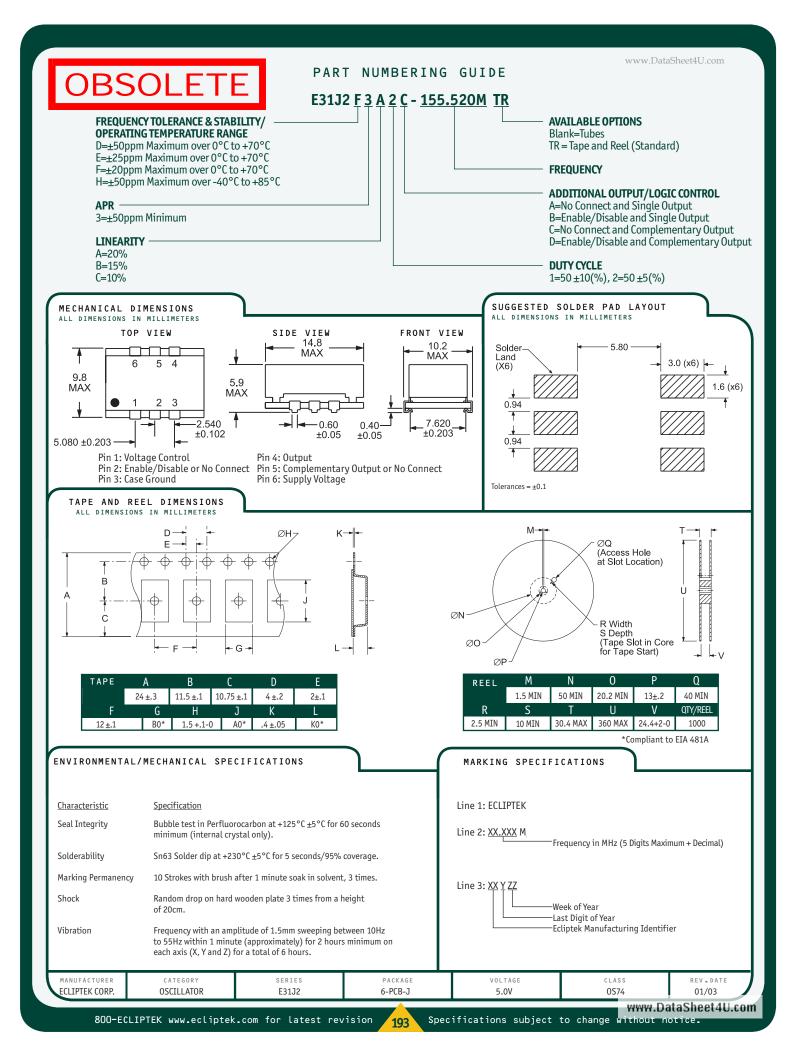
Best Regards,

Mark W Sumer

Mark W. Stoner Director of Marketing Ecliptek Corporation

## E31J2 Series E31J2 PECL Output VCXO • 5.0V supply voltage • 6 pad PCB SMD package with J-leads • Stability to 20ppm • Output Ena D.2 Complement ar Outbur available • Available o Tape and Re OSCILLATOR ELECTRICAL SPECIFICATIONS **Frequency Range** 19.440MHz to 212.500MHz **Operating Temperature Range** 0°C to 70°C or -40°C to 85°C **Storage Temperature Range** -55°C to 125°C Supply Voltage (V<sub>cc</sub>) 5.0V<sub>DC</sub> ±5% **Input Current** 100mA Maximum Logic Type 100KH Frequency Tolerance / Stability Inclusive of Operating Temp Range, Supply Voltage, ±50ppm, ±25ppm, or Load, and Aging @25°C over 10 years ±20ppm Maximum Output Voltage Logic High (V<sub>OH</sub>) $V_{cc}$ -1.025 $V_{DC}$ Minimum Output Voltage Logic Low (V<sub>0L</sub>) V<sub>cc</sub>-1.620V<sub>DC</sub> Maximum **Rise Time / Fall Time** 2 nSeconds Maximum 20% to 80% of waveform **Duty Cycle** at 50% of waveform 50 ±10(%) 50 ±5(%) Load Drive Capability 50 Ohms into V<sub>cc</sub>-2.0V<sub>DC</sub> Additional Output / Logic Control No Connect and Single Output Enable/Disable and Single Output No Connect and Complementary Output or Enable/Disable and Complementary Output Enable/Disable Input Voltage $V_{II}$ of $V_{CC}$ -1.475 $V_{DC}$ Maximum **Enables Output** No Connection **Enables Output** $V_{IH}$ of $V_{CC}$ -1.165 $V_{DC}$ Minimum Disables Output: Logic Low Disables Complementary Output: Logic High **Start Up Time** 10 mSeconds Maximum **RMS Phase Jitter** FJ = 12kHz to 20MHz 1 pSec Maximum Absolute Pull Range (APR) Inclusive of Operating Temp Range, Supply Voltage, ±50ppm Minimum Load, and Aging @25°C over 10 years Linearity 20%, 15%, or 10% Maximum Control Voltage (V<sub>c</sub>): Test Conditions for APR $2.5V_{DC} \pm 2.0V_{DC}$ Control Voltage Range (V<sub>CR</sub>) $0.0V_{DC}$ to $V_{CC}$ **Center Control Voltage** $2.5V_{\text{DC}}$ **Transfer Function** Positive Transfer Characteristic **Input Impedance** 50k0hms Typical **Modulation Bandwidth** 10kHz Minimum at -3dB with Control Voltage of +2.5Vpc CATEGORY MANUFACTURER SERIES PACKAGE VOLTAGE CLASS REV - DATE ECLIPTEK CORP. OSCTLL ATOR 6-PCB-J 01/03 E31J2 5.0V 0S74 www.DataSheet4U.com

800-ECLIPTEK www.ecliptek.com for latest revision Specifications subject to change without notice. 192



## ESTABLE CONFICTION PECL Output VCXO 3.3V supply voltage 6 pad PCB SMD package with J-leads Stability to 20nm Output Engle/Disable available Complementa v Output aviable Available or Tane and Pool

## ELECTRICAL SPECIFICATIONS

Frequency Range					19.440MHz to 212.500MHz		
Operating Temperature	0°C to 70°C or -40°C to 85°C						
Storage Temperature Ra	ange				-55°C to 125°C		
Supply Voltage (V <sub>cc</sub> )					3.3V <sub>DC</sub> ±5%		
Input Current					75mA Maximum		
Logic Type					100KH		
Frequency Tolerance / Stability		Inclusive of Operating Temp Range, Supply Voltage,					
		Load, and A	ging @25°C over 10 ye	ears	±20ppm Maximum		
Output Voltage Logic High (V <sub>OH</sub> )					$V_{cc}$ -1.025 $V_{Dc}$ Minimum		
Output Voltage Logic Lo	ow (V <sub>ol</sub> )				V <sub>cc</sub> -1.620V <sub>DC</sub> Maximum		
Rise Time / Fall Time			20% to 80% of waveform		2 nSeconds Maximum		
Duty Cycle		at 50% of w	at 50% of waveform		50 ±10(%)		
					50 ±5(%)		
Load Drive Capability					50 Ohms into $V_{cc}$ -2.0 $V_{DC}$		
Additional Output / Log	gic Control				No Connect and Single Outpu	ut	
					Enable/Disable and Single O	-	
					No Connect and Complement	tary Output or	
					Enable/Disable and Complem	mentary Output	
Enable/Disable Input Voltage		$V_{IL}$ of $V_{cc}$ -1.475 $V_{DC}$ Maximum		Enables Output			
		No Connect	No Connection		Enables Output		
		$V_{IH}$ of $V_{CC}$ -1.	$V_{IH}$ of $V_{CC}$ -1.165 $V_{DC}$ Minimum		Disables Output: Logic Low		
					Disables Complementary Out	tput: Logic High	
Start Up Time					10 mSeconds Maximum		
RMS Phase Jitter		FJ = 12 kHz	FJ = 12kHz to 20MHz		1 pSec Maximum		
Absolute Pull Range (APR)		Inclusive of	Inclusive of Operating Temp Range, Supply Voltage, ±50ppm Minimum				
		Load, and A	ging @25°C over 10 ye	ears			
Linearity					20%, 15%, or 10% Maximum		
Control Voltage (V <sub>c</sub> ): Test Conditions for APR					1.65V <sub>DC</sub> ±1.35V <sub>DC</sub>		
Control Voltage Range (	$0.0V_{DC}$ to $V_{CC}$						
Center Control Voltage					1.65V <sub>DC</sub>		
Transfer Function					Positive Transfer Characteristic		
Input Impedance					50k0hms Typical		
Modulation Bandwidth		at -3dB wit	at -3dB with Control Voltage of +1.65V $_{\mbox{\tiny DC}}$		10kHz Minimum		
MANUFACTURER CAT	EGORY	SERIES	PACKAGE	VOLTAGE	CLASS	REV DATE	

